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ESTECO INTERNATIONAL USERS' MEETING

Real-Device Real-Time Optimization for Advanced DRAM Circuit Performance

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Product Engineering Analytics

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Agenda

About Micron

Semiconductor Development Challenges

Real-Device Optimization

modeFRONTIER Optimization Result

Summary

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About Micron

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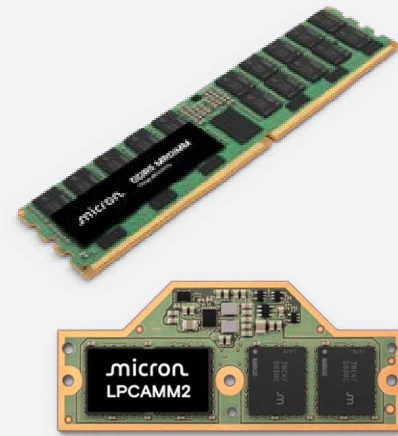
About Micron

Low-power memory

LPDDR5X

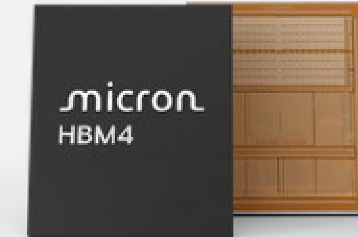


PC memory

DDR5, LPCAMM2

Graphics memory

GDDR7



High-bandwidth memory

HBM4, HBM3E

SSD

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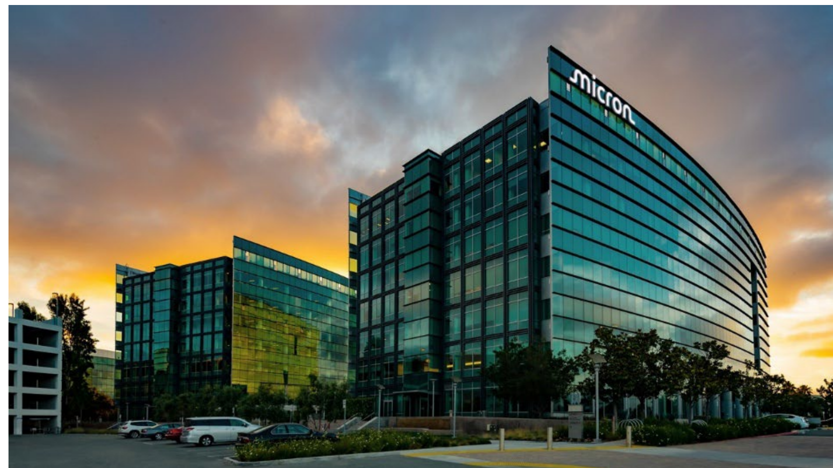
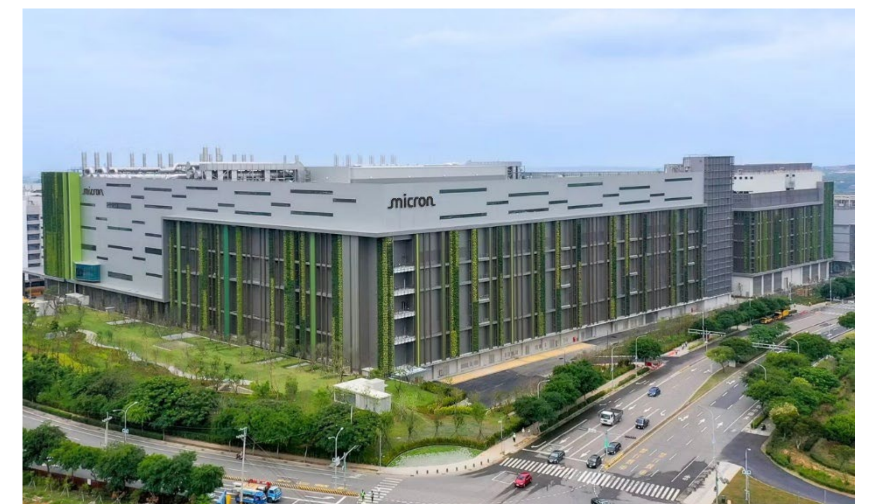
Micron global sites





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We operate across multiple geographic locations worldwide.

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Semiconductor Development Challenges

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Problem Statement

Challenges for the semiconductor industry

01

Complexity

Performance tuning and finding the optimal solution involve a large number of timing and voltage parameters.

02

Variation

Transistor fabrication process on silicon wafers has inherent variation. Performance tuning should address and minimize performance variation as well.

03

Design Change limitations

Design changes are limited by

- Photomask (Reticle)
- Silicon manufacturing process

04

Time Scale (simulation vs. device)

A single functional cycle (~100ns) takes up many hours in large-scale (SPICE) circuit simulation.

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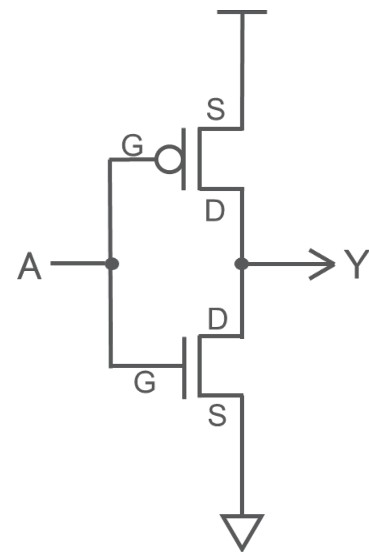
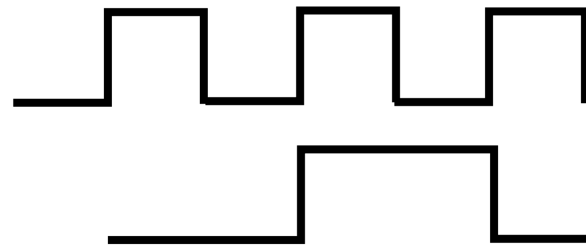
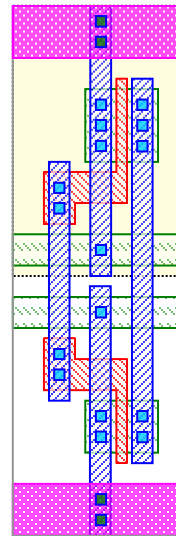
Design Change limitations & Testmode

Circuit Design/Simulation

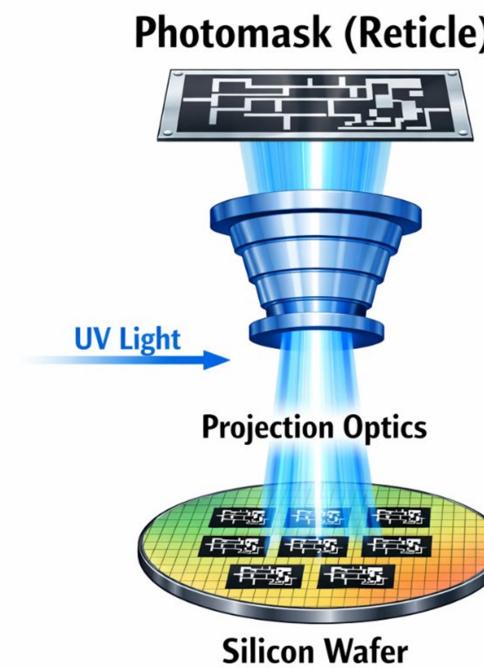




Layout



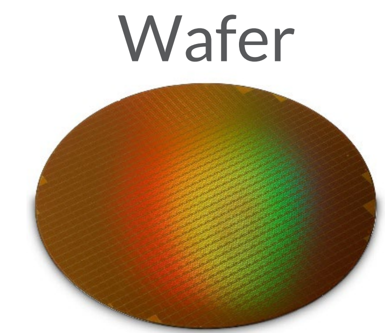
Photomask (Reticle)



⚠ Expensive
⚠ Not revised often

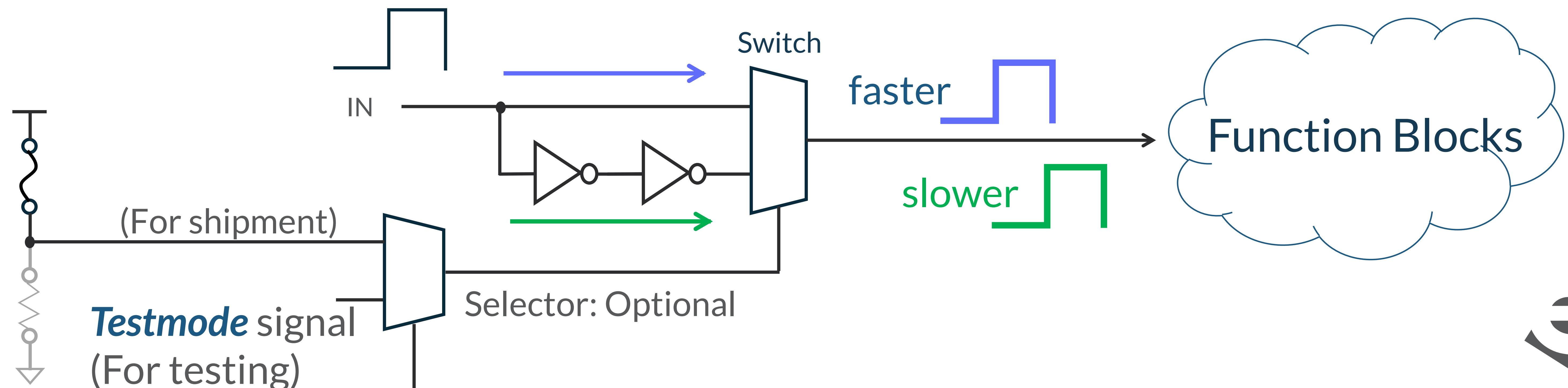
Silicon Process

Wafer



⚠ many weeks, months

Testmode for timing adjustment concept



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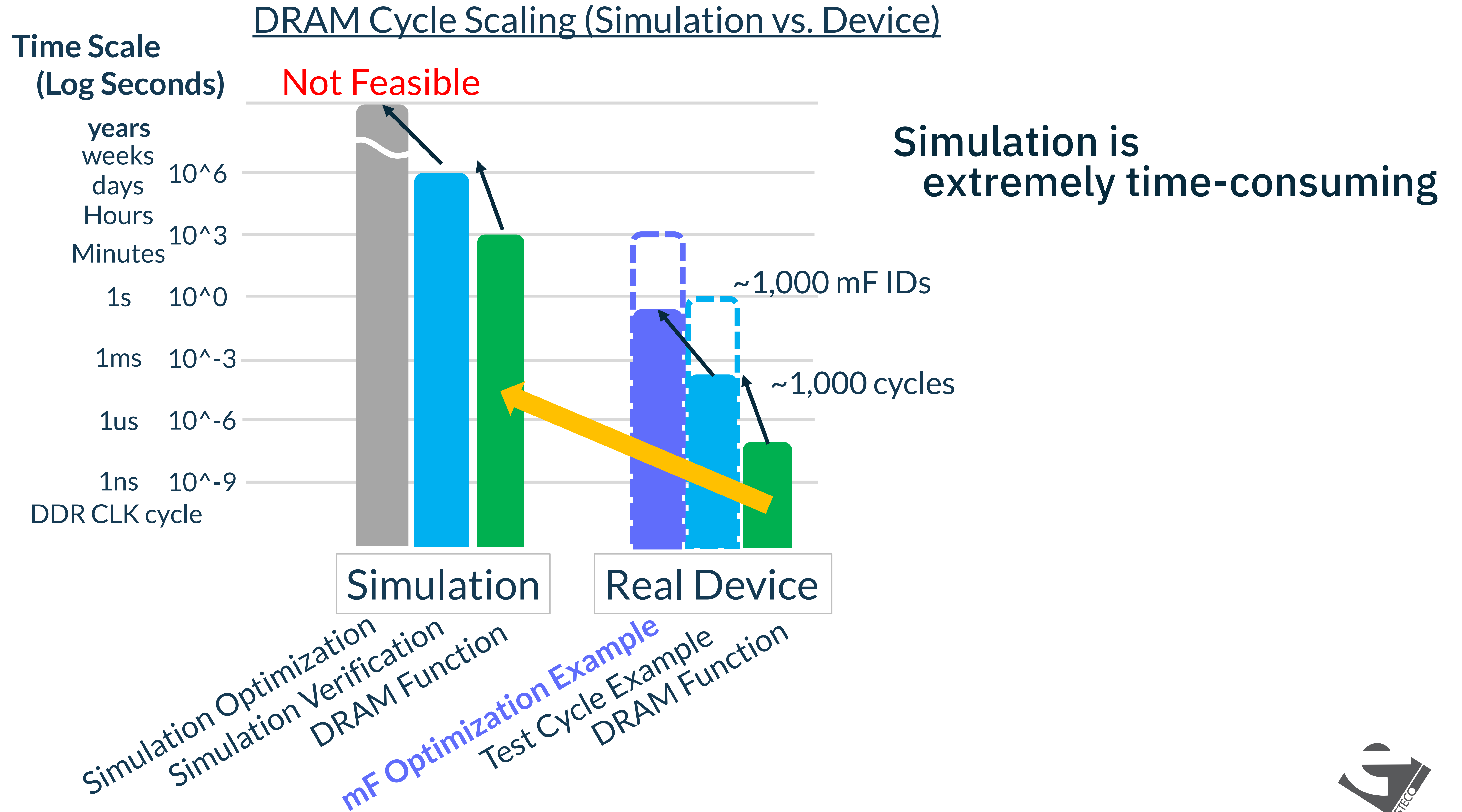
Simulation vs. Real Device



Simulation is
extremely time-consuming

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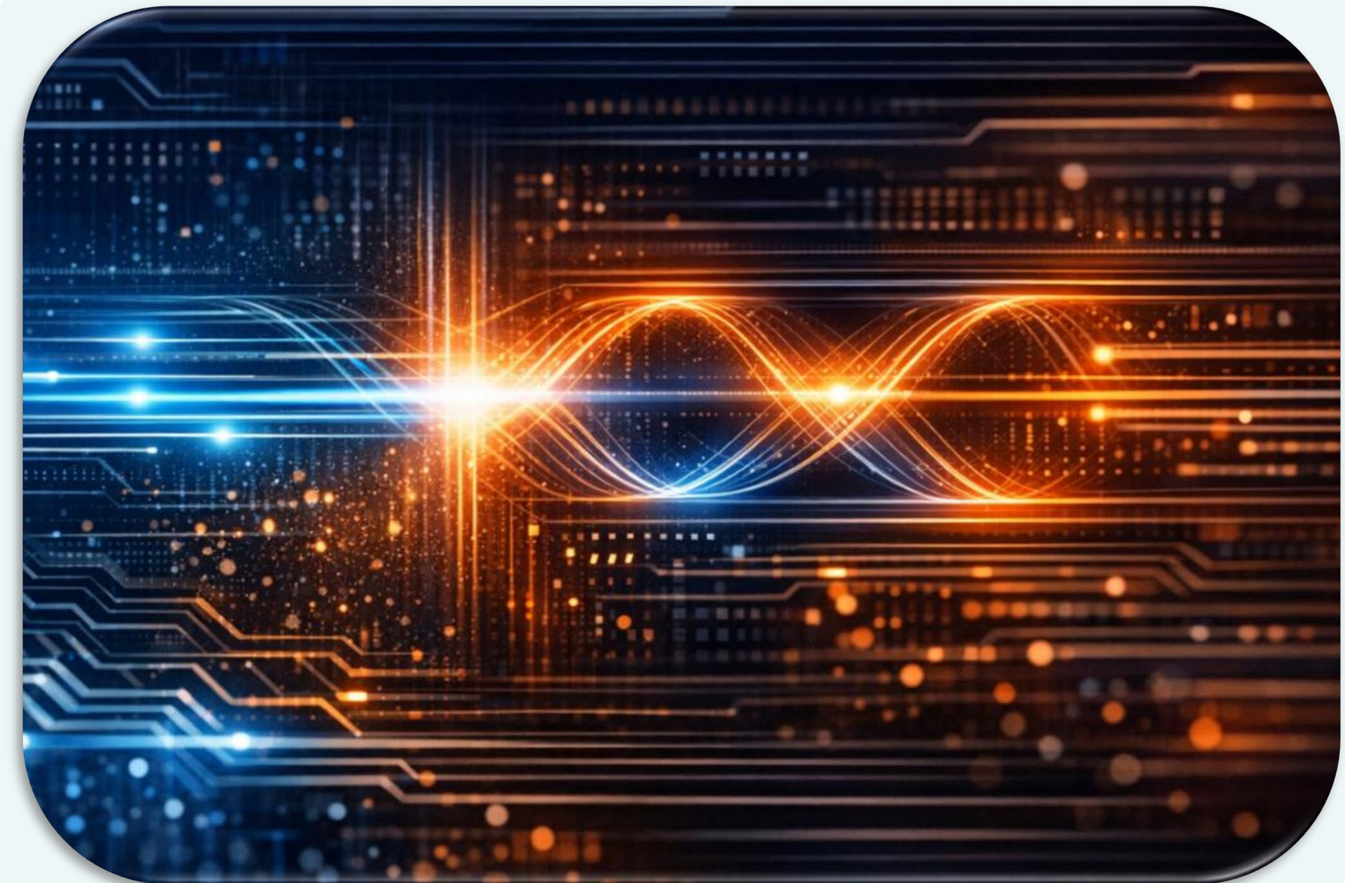
Optimization Targets for Performance

DRAM Function

As the silicon process shrinks, DRAM density grows, memory array operation becomes challenging.
Optimization aims to achieve gigabit-scale tolerance and better yield.



Signal Integrity

DRAM I/O interfaces and internal signals are reaching higher speeds.
Signal quality is critical for achieving high-performance operation.

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Real-Device Optimization

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Our Story

Initial modeFRONTIER Launch:
Time and Performance

Re-optimization

New product
(Parent product)

Conventional Flow

Previous products focused on 5 - 10 parameters.

- Multiple "for loops" with a few parameters.
- or full combination
- Many iterations (data collection & analysis)

On Real Device
On Standalone system

New
Re-design product

New generation model,
Different density,
etc.

modeFRONTIER Flow

New product/application required more parameters at some point.
modeFRONTIER was introduced to address this challenge.
* Server (modeFRONTIER) - client system (real device)

The new redesigned product is similar to previous product optimized by modeFRONTIER. The baseline conditions are carried over from the parent product.

Former product

We no longer use the Conventional Flow
for new products with more parameters.
This study compares approaches by estimating
how many days would have been required using a conventional flow.

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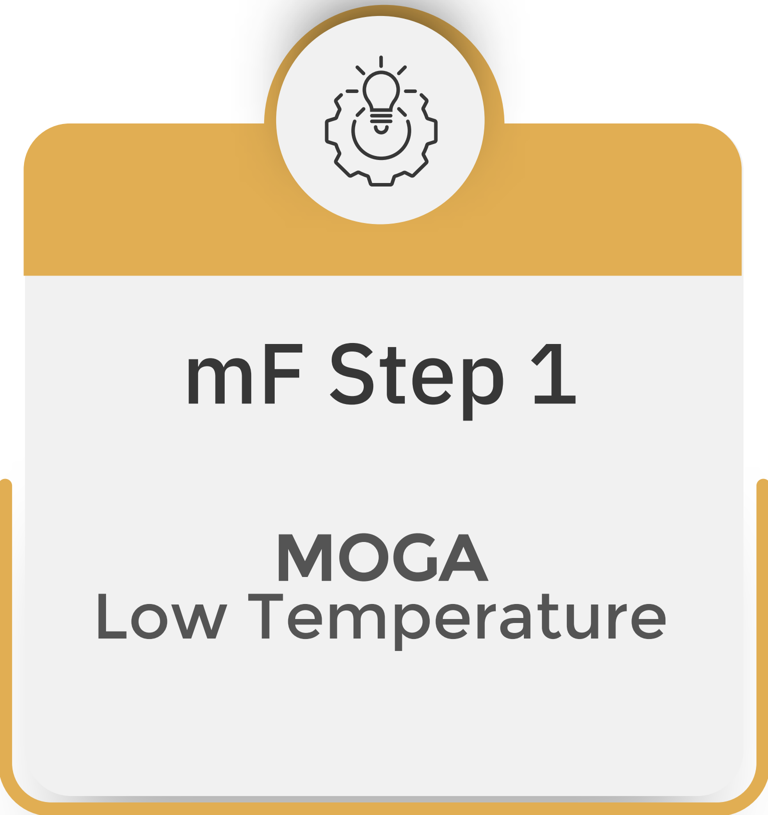
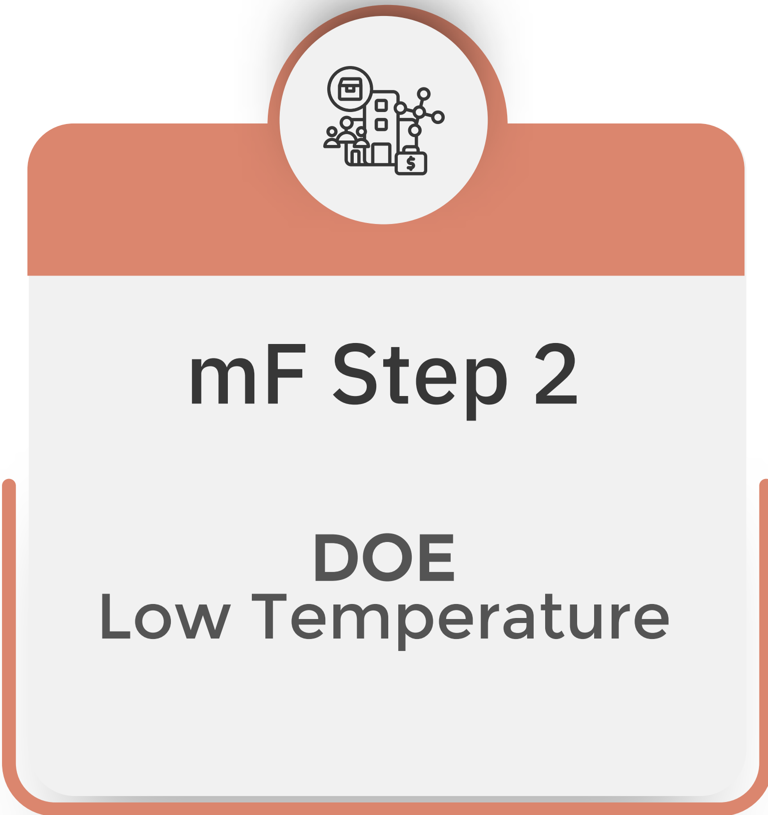
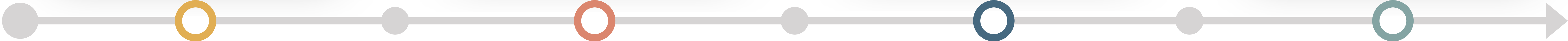
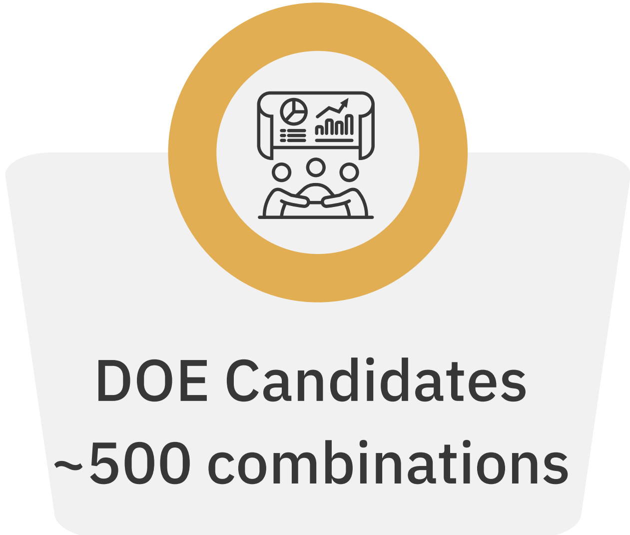
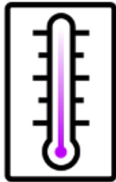
Our Standard Flow (3 Steps)











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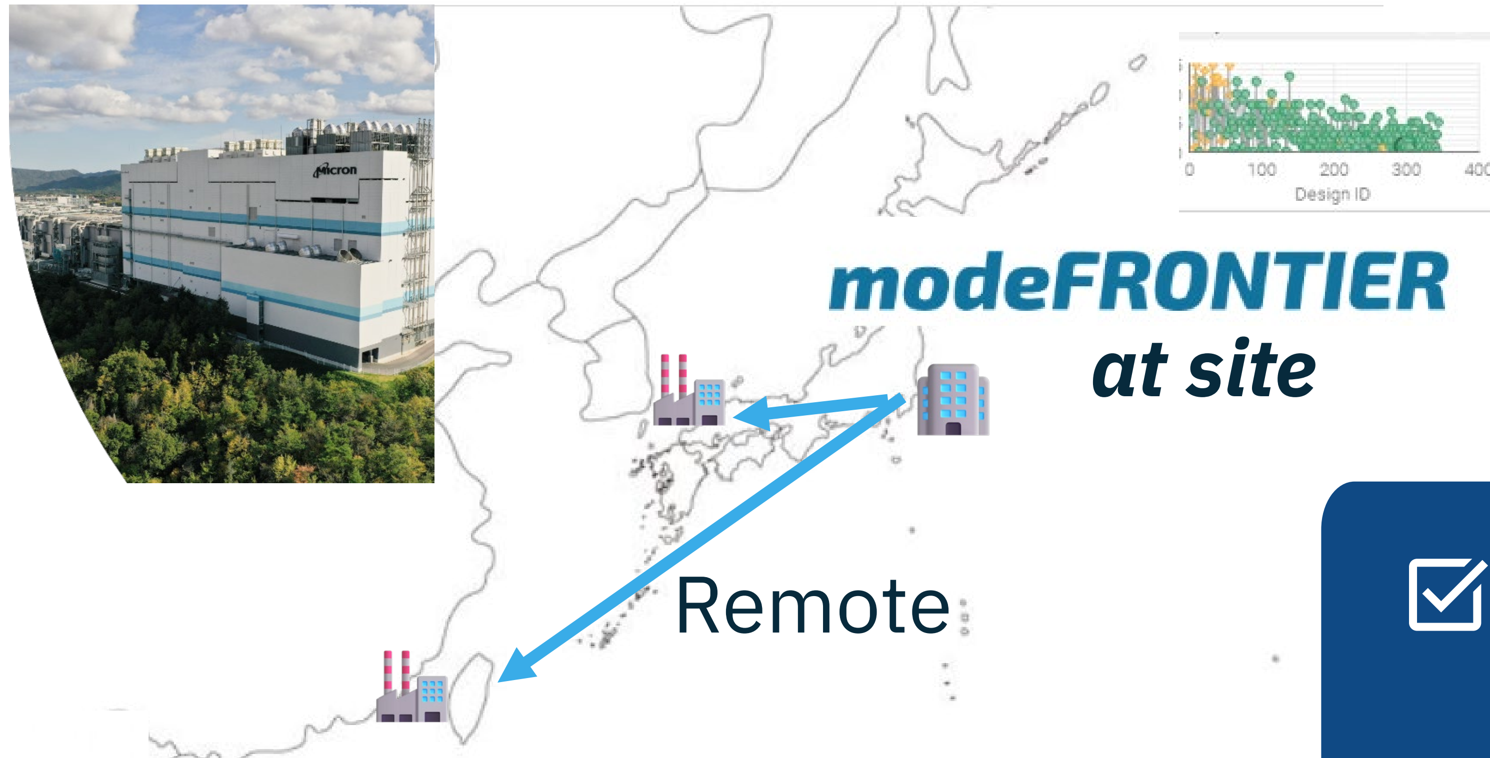
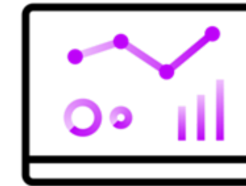
Test to Material with modeFRONTIER

Manufacturing Site



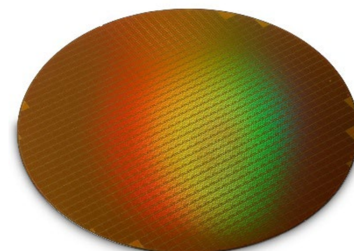


***modeFRONTIER* at site**

Remote

\+ Test Head

\+ Wafer



Wafer Loader / Semiconductor tester

Measurement of hundreds of chips

modeFRONTIER System Enablement Targets

- ☑ Optimize quickly after experimental material available
  - ❌ Avoid sending material to the site
- ☑ Optimize chip variation
  - ❌ Not for the best single chip
- ☑ Optimize parameters for decision-making
  - ❌ Not for post-analysis data collection

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modeFRONTIER Integration Synergy

Optimization and DOE with a Single, Unified Interface

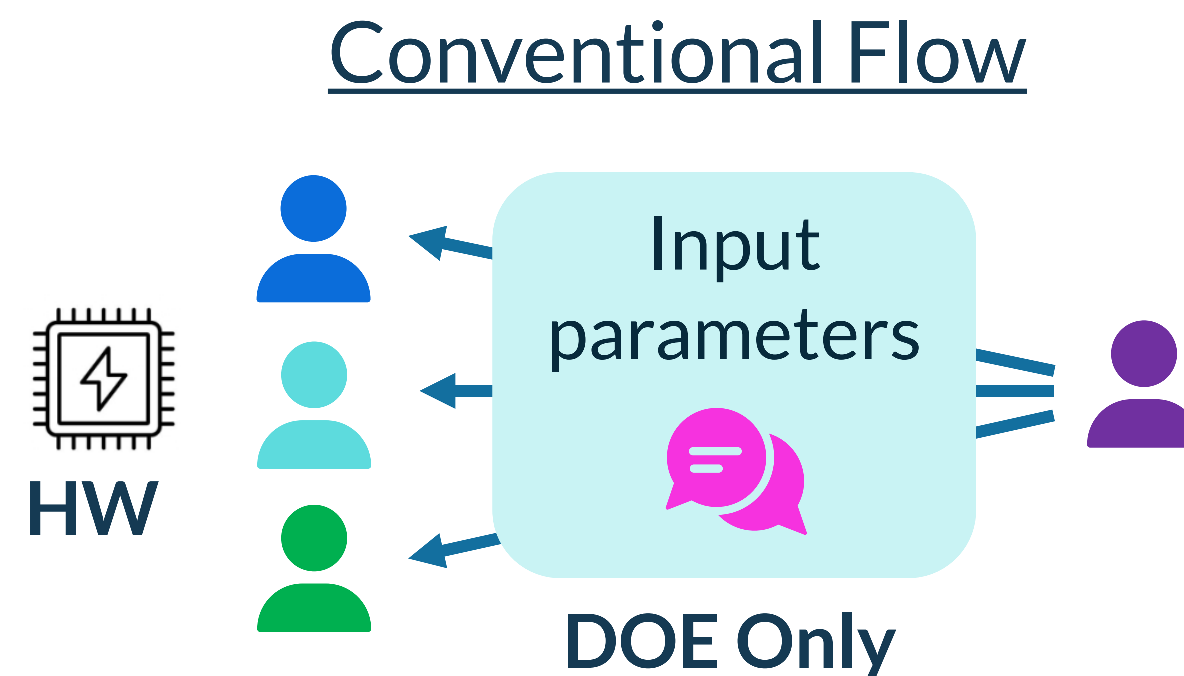
☑ Continuous strong demand for DOE

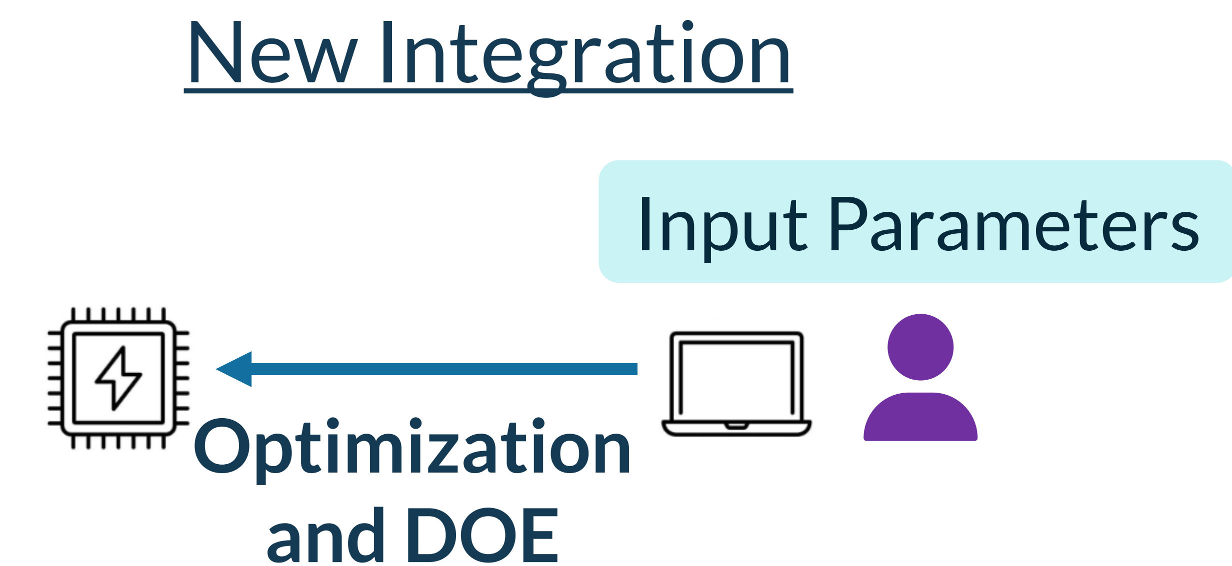
Client (HW) & Server (mF) Style Protocol

☑ No testing requests needed

Isolated Parametric Input Interface

☑ No need to recompile for input requirements





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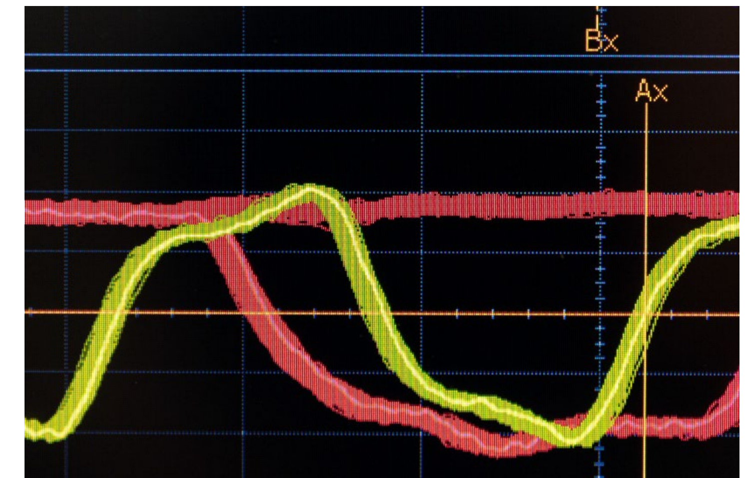
Input Variables

Input Space Example

	Testmode	#of code
1	testmode-A	16
2	testmode-B	4
3	testmode-C	4
4	testmode-D	4
5	testmode-E	8
6	testmode-F	2
7	testmode-G	4
8	testmode-H	...
9	testmode-I	...
10	testmode-J	...
11	testmode-K	...
12	testmode-X	...
13	testmode-Y	...
14	testmode-Z	...
	Total	very large space

Code	Value
0x00	Step 0
0x01	Step +1
0x02	Step +2
0x03	Step +3

Tester and Material



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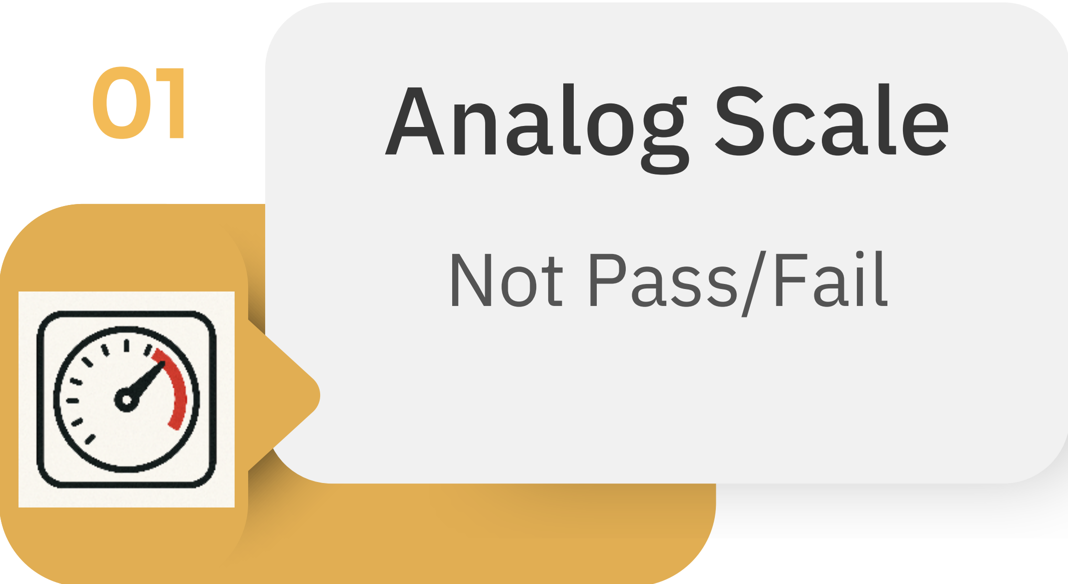
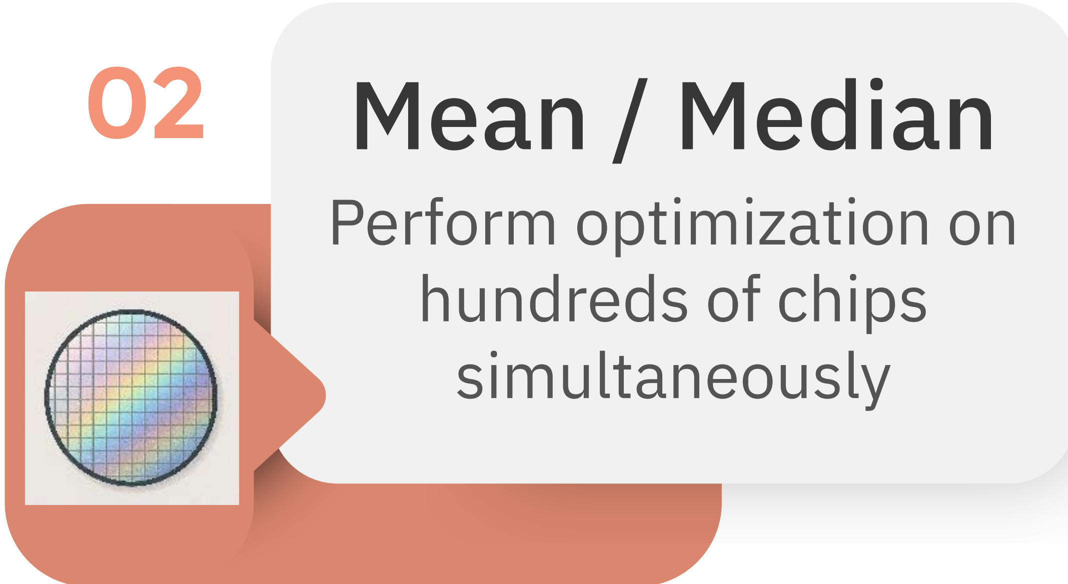
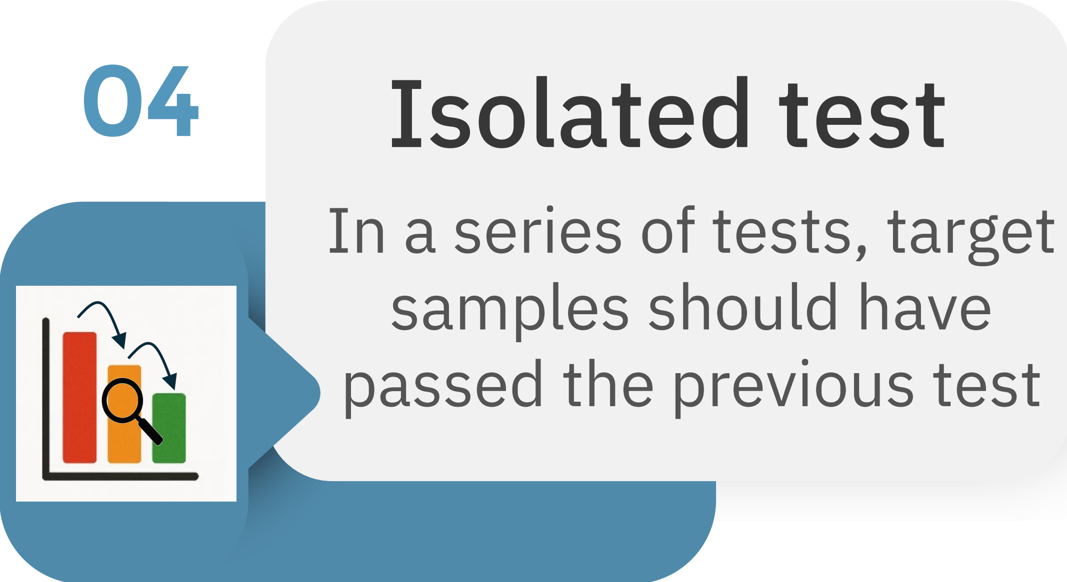
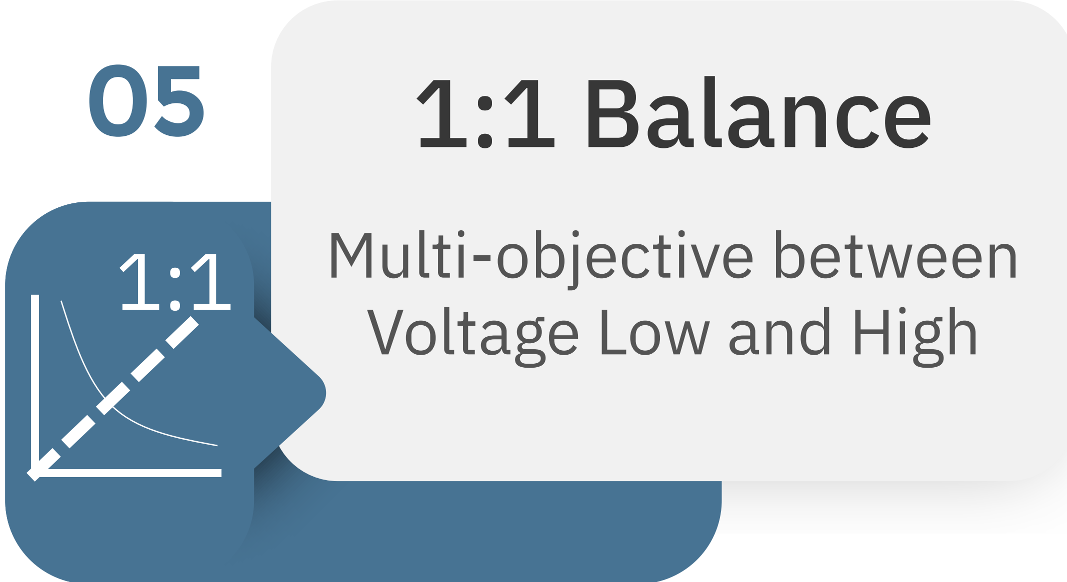
Output Metrics









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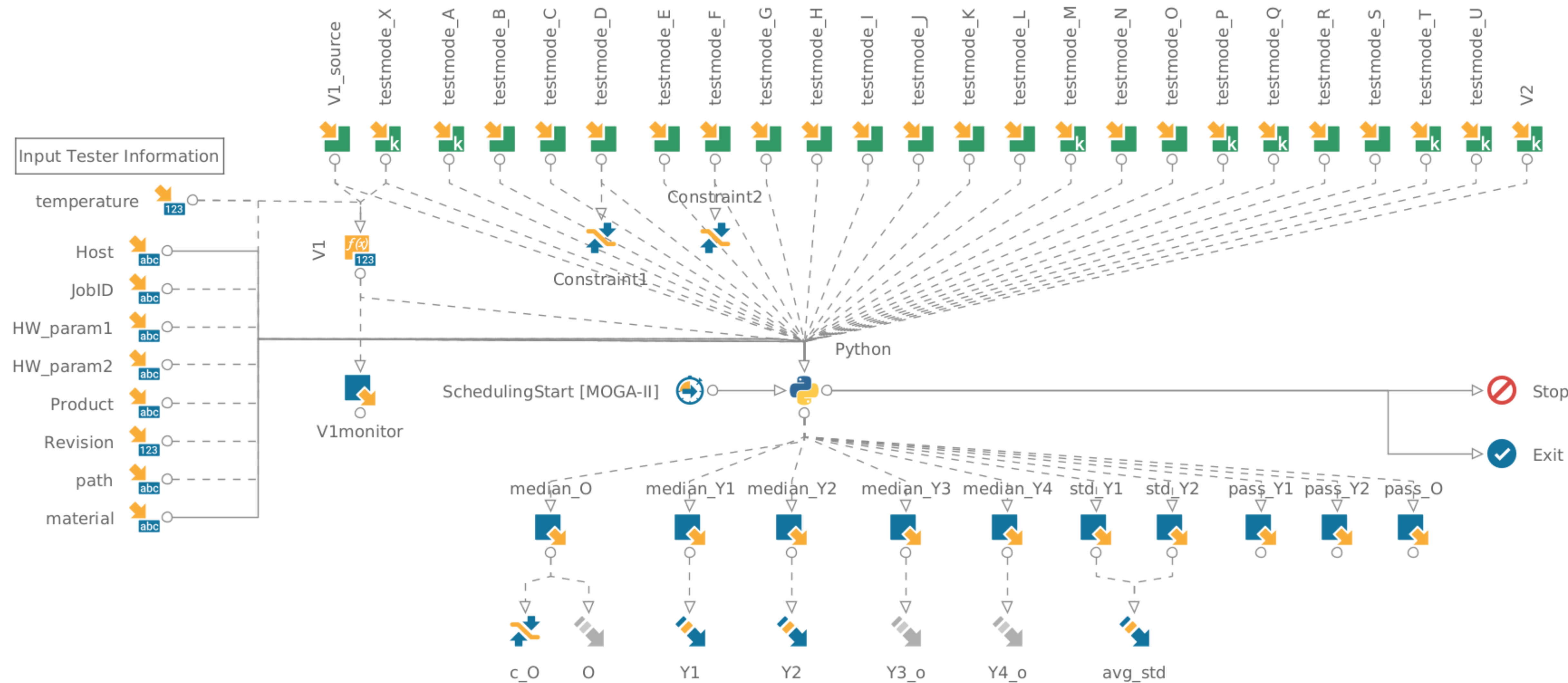
Workflow



20+ Input node

Y1 Y2
Minimize

StdDev
Minimize

- ❑ MOGA-II (Future plan for PilOPT etc.)
- ❑ multi-objective 1:1 balance expectation,
  Optimization of Y1 and Y2
  Legacy concept was to minimize (Y1 + Y2)/2
- ❑ Minimize variation
- ❑ Monitor: Y3 and Y4

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modeFRONTIER Optimization Result

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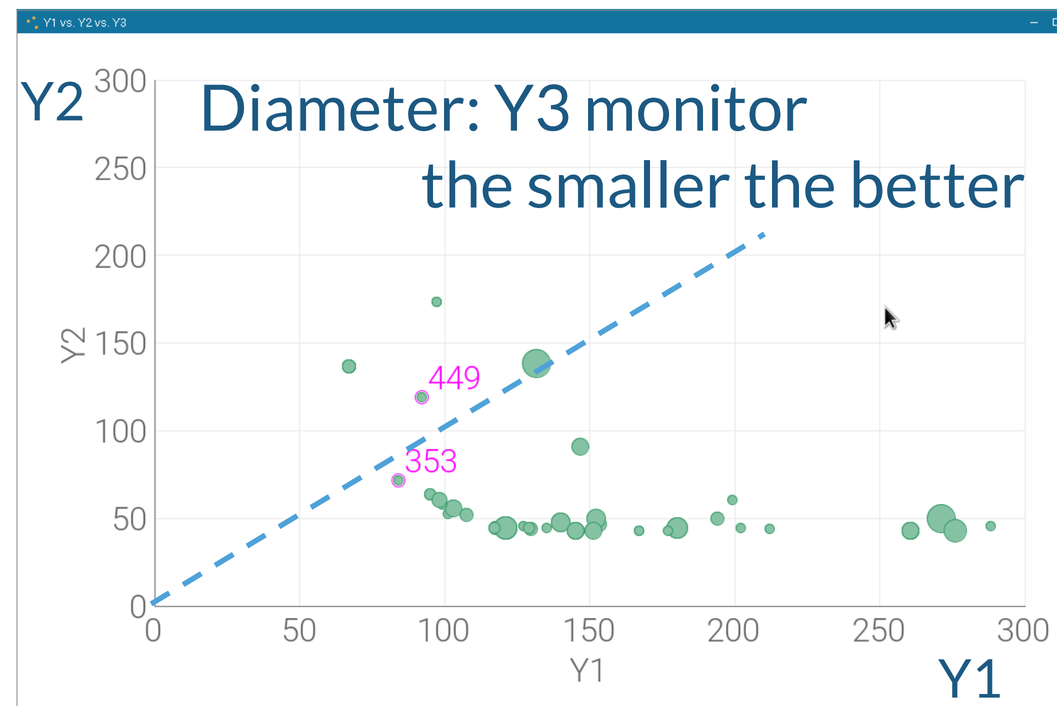
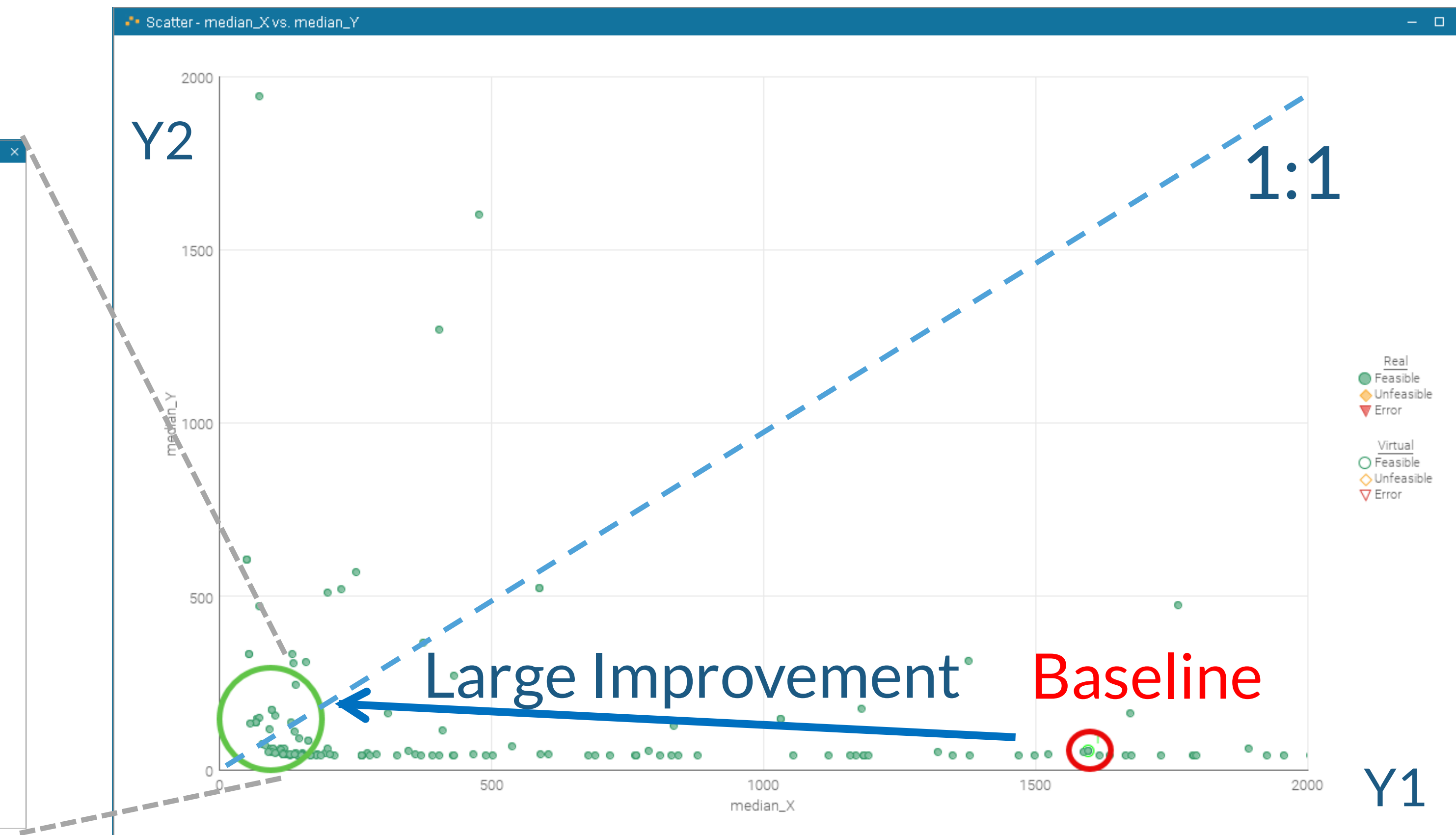
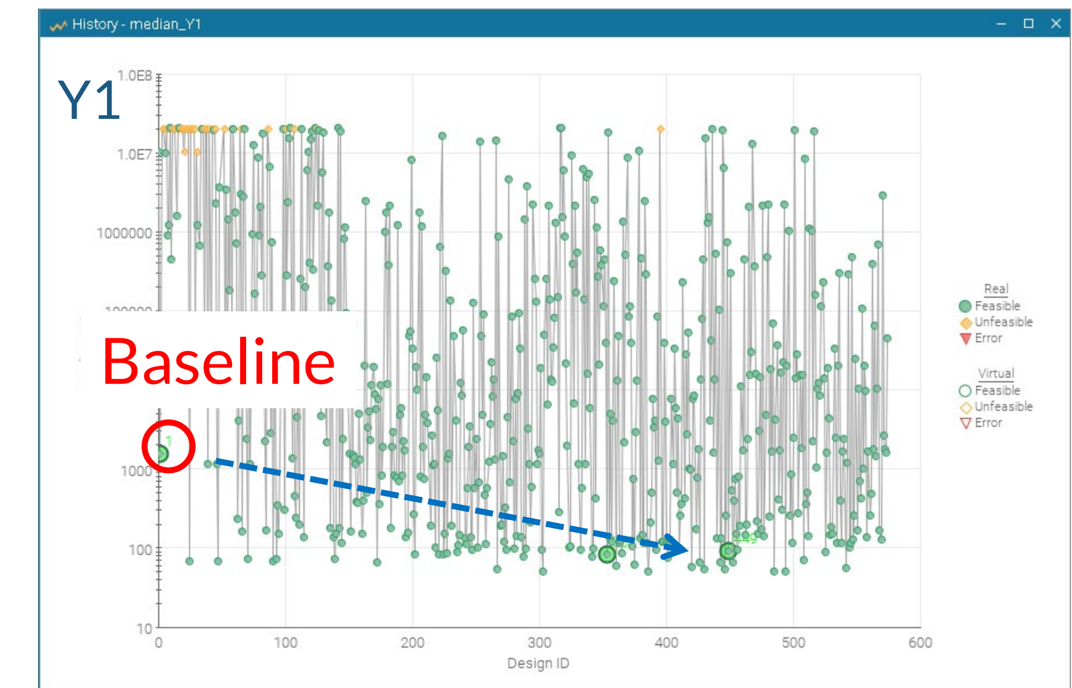
Optimization Results

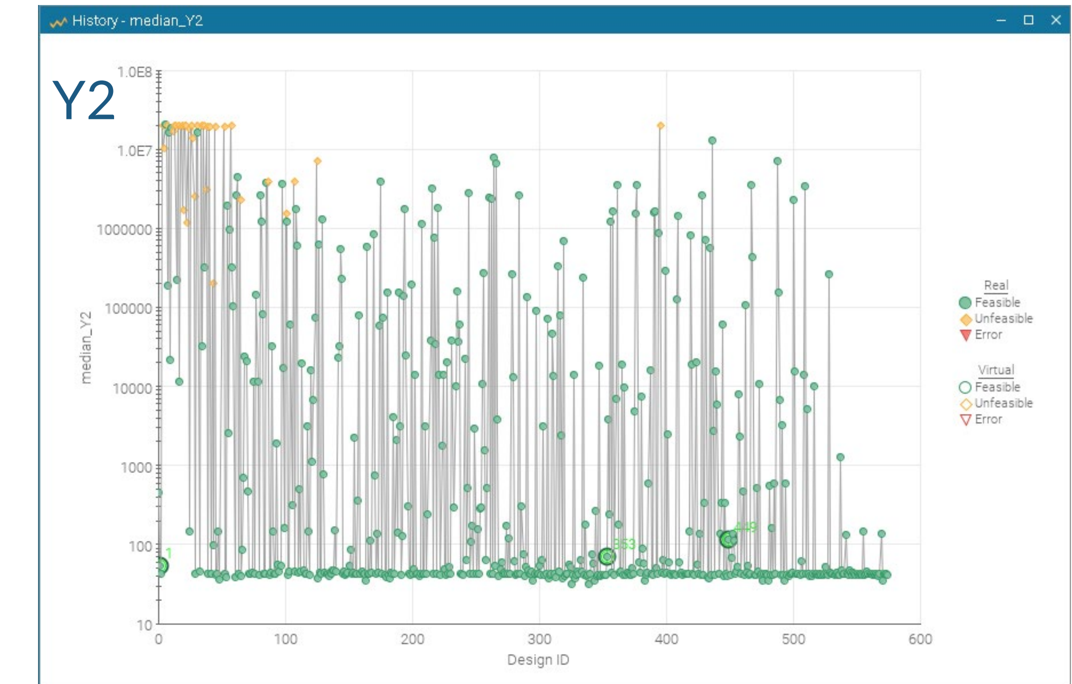


Pareto Front (Zoom)



Pareto Front





History Plot

This product is redesigned from the parent product with some similarity. The best parent product condition is set as the baseline. Performance is recovered, and a 1:1 balance is achieved.

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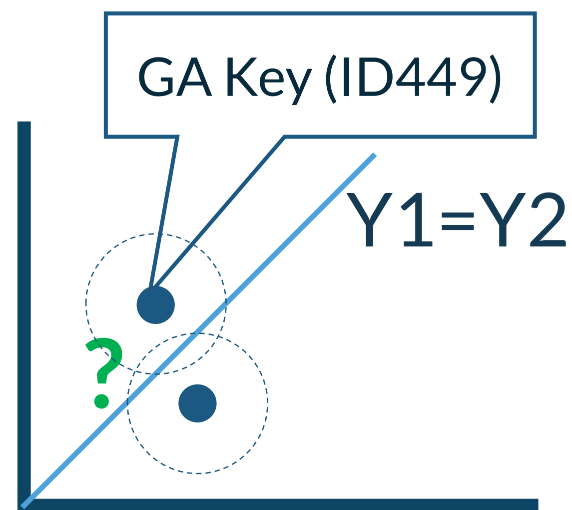
Fine-Tuning (Hot/Cold) How we extend combinational space from the GA best



Any possibilities close to the 1:1 line?

Combinations or Key concepts

	Primary Key	Secondary	
	ID449	ID353	Combinations
Testmode_A	Code 0x01	Code x01	common
Testmode_B	**Code 0x00**	**Code 0x01 ,(0x02)**	**×2 (×3)**
Testmode_C	Code 0x02	Code 0x02	Common
Testmode_D	**Code 0x00**	**Code 0x03**	**×2**
…			…

Up to ~500 combinations (e.g. ×2, ×2, …)

Final Solution by Fine-Tuning

GA Selected

Fine-Tuning

Y1 Y2 Y3 Y4 Std

Final selection

GA Key Selected (ID449)

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Overall Performance and Variation

Chip-level Histogram
with Minimized Mean/Median
and Minimized standard deviation

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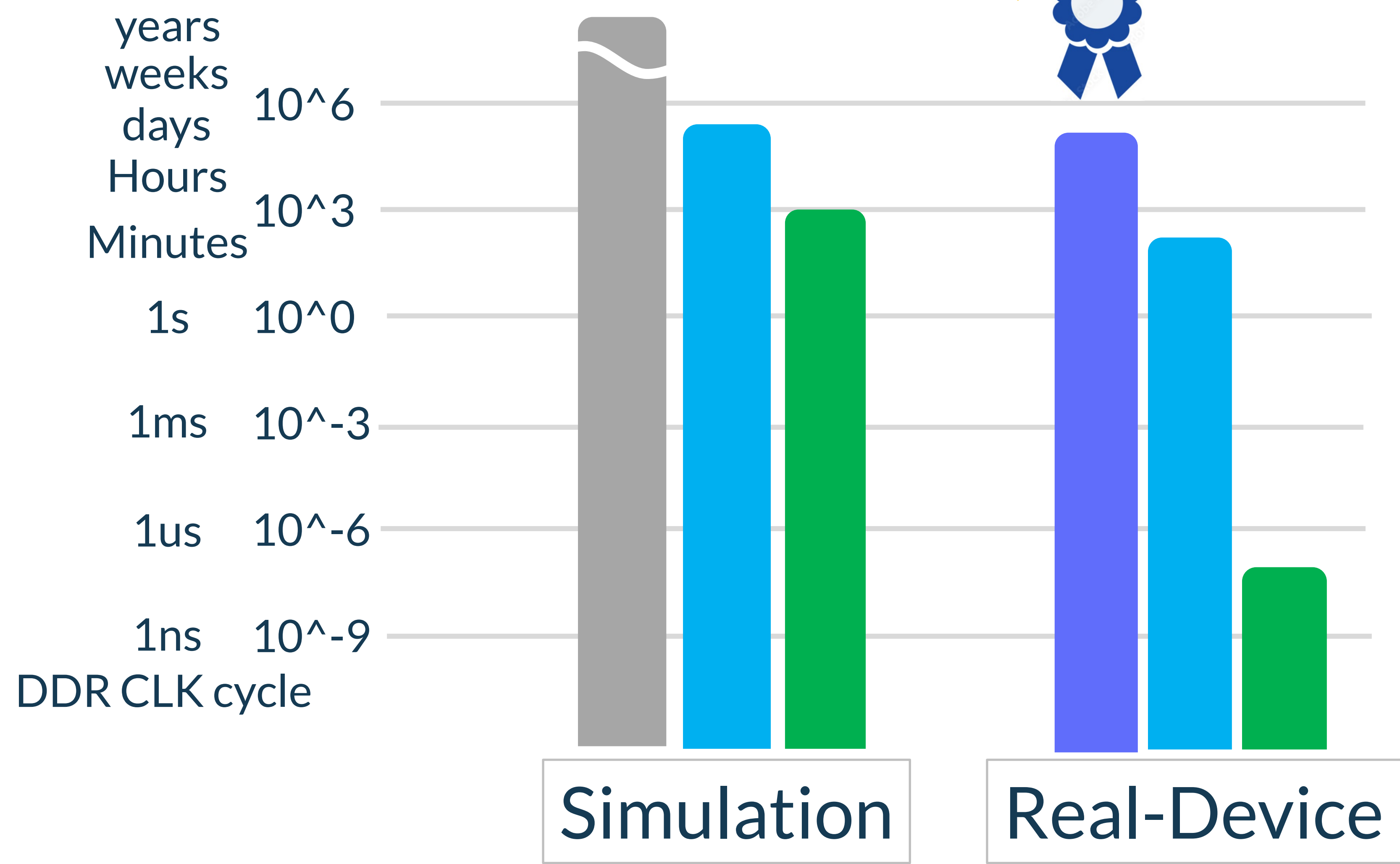
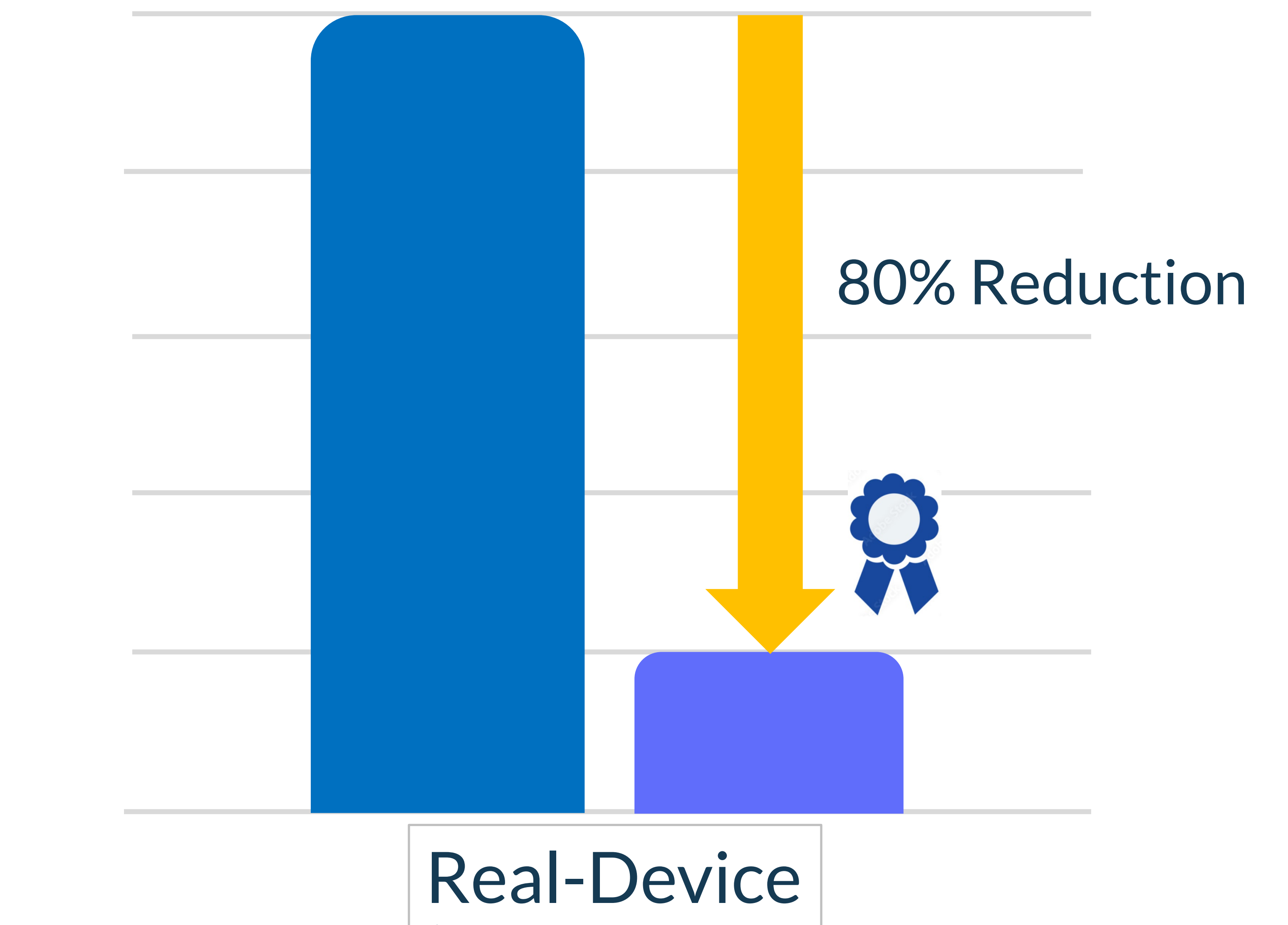
Real-Device Optimization Achievement

DRAM Cycle Scaling (Simulation vs. Device)



Optimization Flow



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Summary

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Summary

- Established **real-device real-time optimization** using modeFRONTIER optimization at Micron.
- **80% time reduction compared to the conventional flow in this phase**
- Performed optimization on hundreds of chips simultaneously with **variation and 1:1 balance**
- Reoptimized quickly across products continuously.
- Eliminated extra workflows and requests required for real-device optimization, enabling fast and direct iteration.

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